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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,216	02/11/2004	Teruo Okada	040057	9967

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EXAMINER
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AMRANY, ADI

ART UNIT	PAPER NUMBER
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2836

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/775,216

Applicant(s)

OKADA ET AL.

Examiner

Adi Amrany

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☒ Claim(s) 8 and 12-16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/18/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Figure 9, item a. Item "a" appears in figure 10 and in the specification is referenced as the signal sampling point located within counter 372 in figure 9 (page 17, line 7). Sampling point "b" is labeled in both figures 9 and 10. It is requested that item "a" be added to figure 9. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

2. The disclosure is objected to because of the following informalities:

a. Beginning on page 6, and continuing throughout the application, voltage-up-down control circuit 200-1 is repeatedly labeled 200. Further, on page 12,

and throughout, control circuit 300-1 is repeatedly labeled 300. The same component must be referred to consistently throughout the application.

- b. Page 6, line 22, "T1" should be inserted after "the terminal,"
- c. Page 6, line 23, "CLK" should be inserted after "oscillation output terminal,"
- d. Page 6, line 24, "HLT" should be inserted after "fault terminal,"
- e. Page 7, paragraph 2, is a run-on sentence that is hard to follow. Please consider making the following revision: "Basic operation of the voltage-up-down control circuit 200-1 involves controlling the drive circuit 204 according to the signal generated by the oscillator 201 and outputting a switching signal from terminal Tsw. The output switching signal controls the switching of the converter in the power source circuit in which the voltage-up-down control circuit 200-1 is located."
- f. Page 7, lines 12-13, it is unclear what applicant means by "generates a reference voltage for *causing the operation* of the voltage-up-down control circuit."
- g. Page 8, line 13, the numerous use of the base word "switch" makes the sentence awkward. Please consider the following revision: "a switch element SW1, which is triggered by the output signal at terminal Tsw..." This phrase recurs several times in the application.
- h. Page 10, line 5, the voltage-down power source is incorrectly labeled. Please change 20-4 to 30-4.

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- i. Page 12, line 20, a "t" in 'the', and a "2" after FIG are missing.
- j. Page 13, line 3, the word "oscillator" is missing before label 301. Please also correct on page 13, line 12.
- k. Page 13, line 8, the drive circuit is incorrectly labeled. Please change 204 to 304.
- l. Page 15, line 5, the numerous use of the base word "switch" makes the sentence awkward. Please consider the following revision: "If an abnormality is detected in either the synchronous line monitor 350 or the power source monitor 352, the mode switches 360, 362, 364 are triggered, and the converter is deactivated."
- m. Page 16, line 6, the phrase "switching of the power source circuit (slave) 30-2 is *carried out in the form* synchronized with the switching frequency" is unclear. Please consider making the following revision: "the power source circuit (slave) 30-2 is synchronized *with* the switching frequency," or "...is synchronized *to* the switching frequency."
- n. Page 16, line 30, "350" should be inserted after "synchronous line monitor."

Appropriate correction is required.

- 3. The abstract of the disclosure is objected to because of improper wording. The object is missing after the verb "enables" in line 1. Please consider the following the revision: "apparatus enables each output to optimize efficiency and to perform simultaneous shutdown." Correction is required. See MPEP § 608.01(b).

***Claim Objections***

4. Claims 8 and 12-16 are objected to because they recite the limitation "abnormality signal," for which there is insufficient antecedent basis.

With respect to claim 8, the limitation "abnormality signal" on line 4 was not disclosed in claims 5 or 6, upon which claim 8 is dependent.

With respect to claim 12, the limitation "abnormality signal" on line 11 was not previously disclosed as an element of claim 12.

Furthermore, dependent claims 13-16 are objected to because they are dependent on base claim 12.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 4-6, and 8-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Tominaga (US 5,237,208).

With respect to claim 1, Tominaga discloses a multiple output power source apparatus (figure 1) comprising:

a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9) equipped with independent output control circuits (figure 2, and column 5, lines 22-26),

wherein the power source circuits equipped with independent output control circuits respectively comprises: abnormality signal output means (figure 2, item 34, and column 6, lines 9-13) for conducting operation shutdown of own circuit (column 5, lines 56-68) when an abnormality occurs in the own circuit and for outputting an abnormality signal to other power source circuits (column 6, lines 9-13).

With respect to claim 2, Tominaga discloses the multiple output power source apparatus according to claim 1, and further discloses an abnormality signal input means (figure 3, column 6, lines 14-22, and column 6, line 46 to column 7, line 5) for inputting the abnormality signal outputted from other power source circuit, and operation shutdown means (figure 3, and column 7, lines 6-29) for conducting the operation shutdown of the own circuit by the input of the abnormality signal by the abnormality signal input means.

With respect to claim 4, Tominaga discloses the multiple output power source apparatus according to claim 2, and further discloses the operation of a power source circuit selected from the plurality of power source circuits equipped with the independent output control circuits is continued by the independent output control circuit even when the abnormality signal has been outputted from the other power source circuits (column 6, lines 56-61). The power source circuits can be set to shut down when any

combination of other power source circuits fail. This includes keeping a power source circuit active even though any number of other power source circuits have failed.

With respect to claim 5, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9) equipped with independent output control circuits (figure 2, and column 5, lines 22-26), wherein the power source circuits comprise synchronous oscillation signal output means (column 7, lines 33-42) for outputting a synchronous oscillation signal synchronized with the switching oscillation frequency of own circuit to output control circuits of other power source circuits.

With respect to claim 6, Tominaga discloses the multiple output power source apparatus according to claim 5, and further discloses a synchronous oscillation signal input means (figure 4, and column 7, lines 43-48) for inputting a synchronous oscillation signal outputted from the other power source circuit, and control means (column 7, lines 49-58) for conducting synchronous control of a switching oscillation frequency used in output control of the own circuit by inputting the synchronous oscillation signal by the synchronous oscillation signal input means.

With respect to claim 8, Tominaga discloses the multiple output power source apparatus according to claim 6, and further discloses the operation of a power source circuit selected from the plurality of power source circuits is continued (column 6, line 46 to column 7, line 5, namely column 6, lines 56-61) by the independent output control circuit even when the abnormality signal has been outputted from the other power

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source circuits. A power source circuits can be kept active even though any number of other power source circuits have failed, as discussed above.

With respect to claim 9, Tominaga discloses the multiple output power source apparatus according to claim 6, and further discloses a control means (column 7, lines 43-55) for synchronously controlling a switching phase used for output control of the own circuit by a switching phase of the synchronous oscillation signal by the synchronous oscillation signal input means.

With respect to claim 10, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9), wherein;

at least two of the plurality of power source circuits are connected by a synchronous line (figure 2, item 20, and column 5, lines 22-26),

first and second power source circuits connected by the synchronous line comprise independent control circuits (figure 2, and column 5, lines 22-26), respectively,

the control circuit provided in the first power source circuit comprises:

synchronous signal output means (column 7, lines 33-42) for outputting a synchronous signal synchronized with the switching frequency of own circuit to the synchronous line,

abnormality signal output means (figure 2, item 34, and column 6, lines 9-13) for outputting an abnormality signal indicating the abnormality occurrence in the own circuit to the synchronous line,

the control circuit provided in the second power source circuit comprises:

synchronous signal input means (column 7, lines 43-55) for inputting the synchronous signal outputted to the synchronous line into the own circuit, and

abnormality signal input means (column 6, lines 14-23) for inputting the abnormality signal outputted to the synchronous line into the own circuit.

With respect to claim 11, Tominaga discloses the multiple output power source apparatus according to claim 10, and further discloses

the control circuit provided in the first power source circuit further comprises abnormality signal input means (column 7, lines 1-5) for inputting the abnormality signal outputted to the synchronous line into the own circuit,

the control circuit provided in the second power source circuit further comprises abnormality signal output means (column 6, lines 46-68) for outputting the abnormality signal indicating the abnormality occurrence in the own circuit to the synchronous line, and

the first and second power source circuits shut down (column 7, lines 6-29) the own circuits when the abnormality signal has been inputted from the synchronous line.

With respect to claim 12, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9), wherein;

at least two of the plurality of power source circuits are connected by a synchronous line (figure 2, item 20, and column 5, lines 22-26),

first and second power source circuits connected by the synchronous line comprise independent control circuits (figure 2, and column 5, lines 22-26),

the control circuits provided in the first and second power source circuits respectively comprise:

frequency synchronization means (figure 2, item 27, and column 5, lines 50-56, and column 7, lines 43-58) for controlling switching frequency of own circuit by using a synchronous signal outputting to the synchronous line, and

abnormality signal detection means (column 8, lines 29-34) for detecting the abnormality signal outputted to the synchronous line and shutting down the own circuit.

With respect to claim 13, Tominaga discloses the multiple output power source apparatus according to claim 12, and further discloses;

the synchronous signal comprises a clock signal (column 5, lines 49-55) of a predetermined frequency,

the abnormality signal is generated by changing the clock signal (column 8, lines 5-34, namely lines 29-34),

the abnormality signal detection means detects change of the clock signal (column 5, lines 56-63).

With respect to claim 14, Tominaga discloses the multiple output power source apparatus according to claim 13, and further discloses the change of the clock signal is generated by the first power source circuit and/or second power source circuit (column 8, lines 5-34, namely lines 18-23).

With respect to claim 15, Tominaga discloses the multiple output power source apparatus according to claim 13, and further discloses the change of the clock signal is implemented by stopping the clock signal (column 6, line 62 to column 7, line 5), and the abnormality signal detection means measures an interval during which the clock signal is stopped and shuts down the own circuit when it is detected that the stop state continues for a predetermined interval or longer (column 7, lines 23-29). Tominaga discloses that AND circuits output a control signal to the mode control circuit. This control signal is "0" or "off" when any number of the detection output signals from the power supply circuits are abnormal. An abnormal signal includes the absence of a signal, which would occur when the oscillator is stopped.

With respect to claim 16, Tominaga discloses the multiple output power source apparatus according to claim 13, and further discloses the change of the clock signal is implemented by changing a voltage level of the clock signal (column 8, lines 18-23) and the abnormality signal detection means measures the voltage level of the clock signal (column 8, lines 29-34) and shuts down (column 8, lines 32-34, release of failure signal "F") the own circuit when a predetermined voltage level is detected. Tominaga

discloses that the outputs of the oscillators are passed through an AND circuit. The AND circuit detects any deviation among the plurality of oscillating signals and if one is detected outputs a parallel release signal. A deviation includes a change in voltage, a change in frequency, or any change that will trigger the AND circuit.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tominaga in view of Luo (US 2005/0073783).

Tominaga discloses the multiple output power source apparatus according to claims 1 and 2, as discussed in the 102(b) rejection above.

Tominaga does not expressly disclose that the abnormality signal output means and the abnormality signal input means conduct input and output of the abnormality signal by using a single terminal.

Luo discloses a multiple output power source (figure 1) comprising a plurality of power source circuits (figure 1, items 10, 101-10N, and paragraph 32, lines 1-3) equipped with independent output control circuits (figures 3A and 3B, and paragraph 38), wherein the abnormality signal output means and the abnormality input means conduct input and output of the abnormality signal by using a single terminal (figure 1,

"comm line" 23 connects to each power source circuit at a single terminal, and paragraph 36).

Tominaga and Luo are analogous art because they are from the same field of endeavor, namely parallel power systems.

At the time of the invention by applicant it would have been obvious to a person of ordinary skill in the art to combine the input monitoring circuit and operation mode monitoring circuit disclosed in Tominaga with the single communication terminal disclosed in Luo.

The motivation for doing so would have been to reduce the number of terminals on the power sources and to reduce the length of transmission wire required to transmit the abnormality signal.

With respect to claim 7, Tominaga discloses the multiple output power source apparatus according to claims 5 and 6, as discussed in the 102(b) rejection above.

Tominaga does not expressly disclose the synchronous oscillation signal output means and the synchronous oscillation signal input means conduct input and output by using a single terminal.

Luo discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 10, 101-10N, and paragraph 32, lines 1-3) equipped with independent output control circuits (figures 3A and 3B, and paragraph 38), wherein the synchronous oscillation signal out means and the synchronous oscillation input means conduct input and output by using a single terminal

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(figure 1, "sync" line connects to each power source circuit at a single terminal, and paragraph 35).

Tominaga and Luo are analogous art because they are from the same field of endeavor, namely parallel power systems.

At the time of the invention by applicant it would have been obvious to a person of ordinary skill in the art to combine the AC synchronizing signal disclosed in Tominaga with the single clock terminal disclosed in Luo.

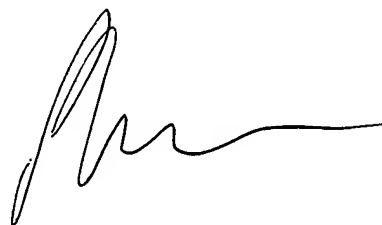
The motivation for doing so would have been to reduce the number of terminals on the power sources and to reduce the length of transmission wire required to transmit the synchronizing signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adi Amrany whose telephone number is (571) 272-0415. The examiner can normally be reached on weekdays, from 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Phuong T. Vu', with a stylized, flowing script.

PHUONG T. VU  
PRIMARY EXAMINER